A Diamond:H/WO$_3$ Metal–Oxide–Semiconductor Field-Effect Transistor

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Abstract—A p-type Diamond:H/WO$_3$ metal–oxide–semiconductor field-effect transistor (MOSFET) based on surface transfer doping is demonstrated. Using a low-temperature ALD-grown HfO$_2$ as gate insulator, the Diamond:H/WO$_3$ MOSFETs show excellent output characteristics, gate-controllable 2-D hole gas, and low gate leakage current. Long-channel FETs exhibit improved subthreshold behavior but reduced transconductance with respect to short-channel devices. An observed WO$_3$-thickness-dependent threshold voltage is consistent with enhanced surface transfer doping as the WO$_3$ layer is thinned down. Low-temperature measurements suggest a significantly lower mobility than expected in this material system. This illustrates the challenge of maintaining high TMO quality during device fabrication.

Index Terms—Diamond:H, gate length, surface transfer doping, temperature, WO$_3$ thickness.

I. INTRODUCTION

DIAMOND is an ultra-stable material with a wide band gap of 5.47 eV. Recently developed surface transfer doping (STD) has opened a new avenue to exploit the excellent electrical and thermal properties of diamond [1]. The negative electron affinity that results after diamond surface hydrogenation (Diamond:H or, simply, D:H) enables the transfer of electrons from Diamond:H to high work-function acceptors located at its surface. This results in the formation of a two-dimensional hole gas (2DHG) at the Diamond:H surface.

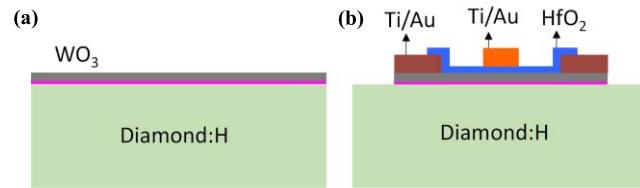Up to this date, water [2], fullerenes (C$_{60}$) [3], fluorinated Fullerenes (C$_{60}$F$_x$, x = 18, 36, 48) [4],

Fig. 1. Schematic cross-section of (a) starting heterostructure and (b) p-type Diamond:H/WO$_3$ MOSFET.

zinc-tetraphenylporphyrin (ZnTPP) coupled C$_{60}$F$_{48}$ [5], Tetrafluoro-tetracyanoquinodimethane (F$_4$-TCNQ) [6], and more recently transition-metal oxides (TMOs) [7]–[10], have been investigated as surface acceptors for D:H. Among these, TMOs such as MoO$_3$, WO$_3$, ReO$_3$ and V$_2$O$_5$, stand out with their unique properties of wide-band gap and high electron affinity. As a typical TMO, MoO$_3$ was first used as acceptor on Diamond:H and metal-oxide-semiconductor field-effect transistors (MOSFETs) have been demonstrated [11]. Separately, MoO$_3$ has also been used as a gate dielectric for Diamond:H MOSFETs [12]. D:H/V$_2$O$_5$ MISFETs have also been reported [13].

Most recently, D:H/WO$_3$ has been found to have enhanced charge-transfer robustness and efficiency [14], as compared to the D:H/MoO$_3$ and D:H/V$_2$O$_5$ systems. A Hall-effect study of thermally-evaporated WO$_3$ on D:H measured a record areal hole carrier concentration of 4.8×10^{14} cm^{-2} at a temperature up to 150°C [14]. The hole mobility reached over 100 cm^{2}V^{-1}s^{-1} for temperatures up to 300°C. In an effort to take advantage of the outstanding charge-transfer properties of this system, in this work we demonstrate the first implementation of a MOSFET in the D:H/WO$_3$ system. Moreover, we investigate the impact of WO$_3$ thickness, gate length and low temperature operation in the device characteristics.

II. DEVICE FABRICATION

Figure 1 shows a schematic cross section of the starting heterostructure and the fabricated MOSFET. Three $3 \times 3 \times 0.5$ mm^3 type IIa (001)-oriented single-crystal diamond substrates supplied from Element6, with nitrogen concentration < 1 ppm were used. Surface hydrogenation was performed by exposure to pure hydrogen plasma in a CVD reactor at 600°C for 40 minutes. Subsequently, the samples were heated at 350°C to desorb H$_2$O molecules and contaminants from the diamond surface in vacuum [11]. This was immediately followed by low-rate (0.1 Å/min) thermal evaporation of different thicknesses (2.4, 3.4 and 4.8 nm) of WO$_3$ in each
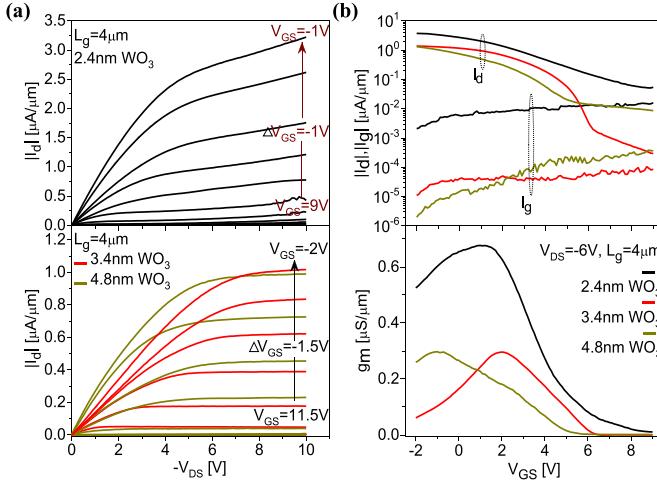
Fig. 2. Output (a) and transfer (b) characteristics for $L_g = 4\ \mu m$ Diamond:H/WO₃ FETs with WO₃ thickness ranging from 2.4 nm to 4.8 nm.

Fig. 3. Electrical characteristics of 4.8 nm-thick WO₃ D:H/WO₃ FETs with gate width of 20 μm and different gate lengths ranging from 0.7 μm to 5 μm: (a) subthreshold and gate current characteristics; (b) g_m characteristics; (c) maximum g_m ($g_{m_{max}}$) and maximum drain current (I_{Dsat}), all at $V_{DS} = -6$ V; (d) ON resistance.

sample. A surface roughness of Ra $\sim$ 0.6 nm over an area of 1 μm $\times$ 1 μm was measured by AFM, and a WO₃ thickness uniformity of 10% was evaluated by ellipsometry. The stoichiometry and thickness of WO₃ was characterized by X-ray photoelectron spectroscopy and ellipsometry and results similar to those reported in Ref 14 were obtained.

The process continues with electron-beam evaporation of Ti/Au (20/200 nm), as source and drain electrodes, through a shadow mask. Following this, 20 nm of HfO₂ as gate dielectric layer was grown by atomic layer deposition (ALD) at 150° C. The use of a gate oxide was deemed essential to obtain a working FET since WO₃ is expected to become highly conductive after the surface transfer process [14]. After that, flowable oxide (FOX) was spin coated on the sample surface and exposed by electron-beam lithography (EBL). This forms a hard mask that is used to define the active channel. Reactive-ion etching based on a BCl₃/Cl/Ar chemistry was performed to etch the exposed HfO₂ and WO₃ and to desorb the Hydrogen from the diamond surface. FOX was then striped with a buffered oxide etchant. Subsequently, a standard photolithographic liftoff step was used to create a Ti/Au (10/100 nm) gate electrode at the center of the channel of the FETs. Devices with gate lengths (L_g) ranging from 0.7 to 5 μm and a constant gate width (W_g) of 20 μm were fabricated. The source-drain distance gradually increased from 29 μm to 58 μm as the gate length changed from 0.7 μm to 5 μm.

In this first demonstration, no effort was given to bringing the source and drain ohmic contacts directly onto the D:H surface. Rather, the goal of this work was to demonstrate the viability of the D:H/WO₃ as a MOSFET system.

III. RESULTS

Fig. 2 shows electrical characteristics of typical MOSFETs with $L_g = 4\ \mu m$ and different WO₃ thickness. All devices show well saturated drain current behavior with sharp pinchoff and low output conductance (Figs. 2a and 2b). The 2.4 nm WO₃ MOSFETs show greater drain current, I_d, and
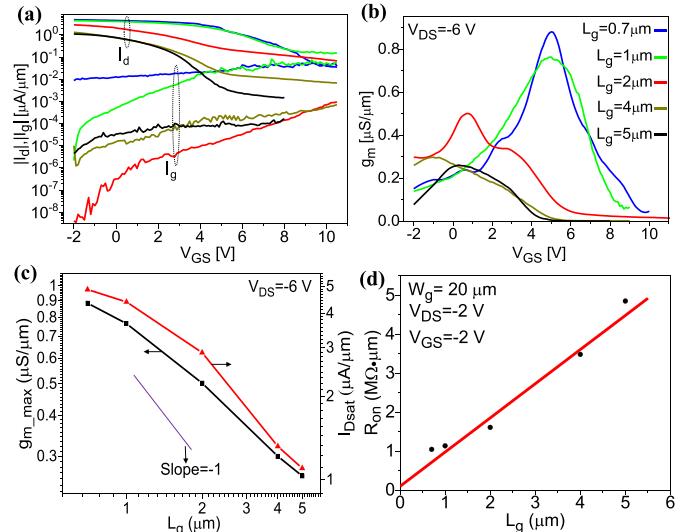
transconductance, g_m (Fig. 2b), and a more positive threshold voltage, V_T. These results are consistent with recent Hall effect observations of decreased surface transfer efficiency and a reduced sheet hole concentration (from 2.5×10^{14} cm^{-2} to 1.3×10^{14} cm^{-2}) of D:H with increasing WO₃ thicknesses (from 1.2 nm to 4.8 nm) [14].

The thinner WO₃ devices also show greater gate leakage current, I_g, (Fig. 2b). This also results in worse drain current saturation (Figs. 2a and 2b). A more effective electron transfer into the 2.4 nm thick WO₃ layer is a plausible explanation for the larger gate current.

We have studied the impact of gate length, L_g, on the electrical characteristics of 4.8 nm-thick WO₃ devices. This is graphed in Fig. 3. Fig. 3a shows that the subthreshold behavior rapidly improves as L_g increases. This probably stems from a combination of short-channel effects and reduced I_g. In addition, we observe a significant improvement in peak transconductance, $g_{m_{max}}$, as L_g decreases (Fig. 3b). The threshold voltage, V_T, shifts positive as gate length shortens. This could be explained by severe short-channel effects that arise from the use of a relatively thick gate dielectric coupled with the absence of body doping [15]. Fig. 3c plots $g_{m_{max}}$ and the maximum drain current, I_{Dsat} as a function of gate length at $V_{DS} = -6$ V. The results indicate both $g_{m_{max}}$ and I_{Dsat} correlate well with each other and scale in a well behaved manner with L_g.

In addition, we extracted the ON resistance of 4.8 nm-thick WO₃ transistors with different L_g at $V_{GS} = -2$ V and and $V_{DS} = -2$ V (Fig. 3d). At this V_{GS}, the ON resistance is largely saturated to its minimum value. From extrapolation of these data to $L_g = 0$, we estimated a total source/drain access resistance of $\sim$197 k$\Omega \bullet \mu$m.

We have also studied the effect of temperature on the electrical characteristics of an $L_g = 5\ \mu$m, WO₃ = 4.8 nm FET at 77 K. The results are presented in Fig. 4. At 77 K, we observe

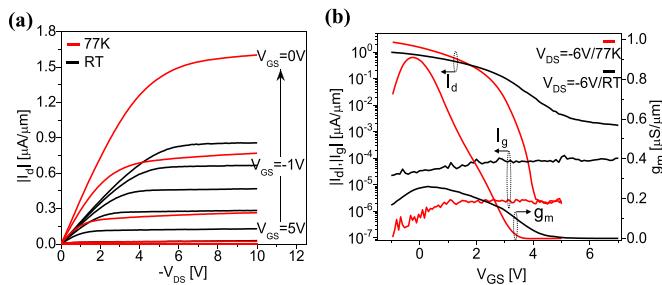Fig. 4.   Output (a) and transfer (b) characteristics for L_g = 5 μm, WO_3 = 4.8 nm Diamond:H/WO_3 FETs measured at 77 K and RT.
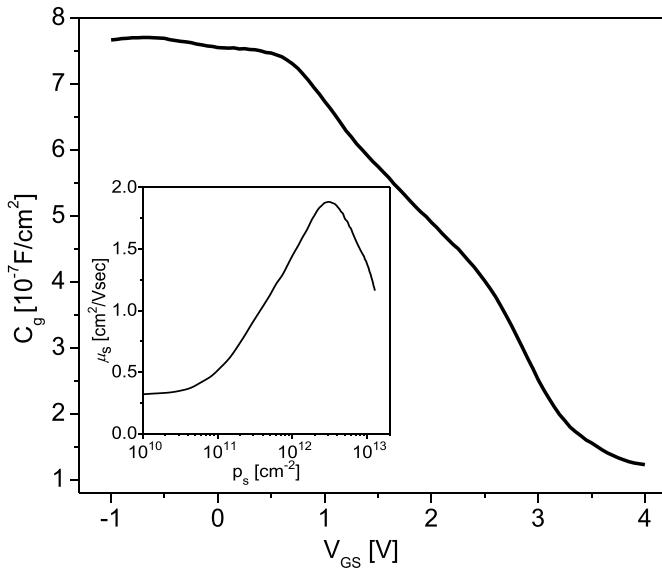

Fig. 5.   Split C-V measurements at 1 MHz of a typical Diamond:H/WO_3 FET (L_g = 5 μm, W_g = 20 μm, WO_3 = 4.8 nm) at 77 K. Inset: sheet hole mobility vs. sheet hole concentration.

a large increase in I_d and g_m with g_{m_max} scaling up by 3.5 times. We also see that I_g was reduced by about two orders of magnitude (Fig. 4b). This results in significantly improved subthreshold behavior with the minimum subthreshold swing (S_{min}) scaling down from $\sim$ 1225 mV/dec to $\sim$ 190 mV/dec and the ON-OFF ratio improving from $\sim 10^3$ to $\sim 10^6$, as the temperature is reduced from RT to 77K.

Device operation at 77 K was further studied by carrying out capacitance-voltage ($C_g - V_{GS}$) and I-V transfer ($I_d - V_{GS}$) characteristics in a device with 4.8 nm of WO_3 and L_g = 5 μm. The C-V characteristics were measured at 1 MHz with V_{DS} = 0 V. $I_d - V_{GS}$ measurements were performed at V_{DS} = -2 V. A typical $C_g - V_{GS}$ result is shown in Fig. 5. From these data, we extract the gate voltage dependence of the sheet hole concentration (p_s) and hole mobility (μ_p) [16], [17]. We also assume that the access resistance does not change with temperature since it is believed to be largely dominated by the contact resistance. We find that, in any case, the extracted mobility exhibits weak sensitivity to the actual value of access resistance that was used.

The inset of Fig. 5 graphs the sheet hole mobility (μ_s) vs. sheet hole concentration (p_s). Over most of its range, the mobility increases with hole concentration. This

suggests that Coulomb scattering dominates at low temperature. We observe a maximum sheet hole concentration of about 3.1×10^{12} cm^{-2}, The corresponding mobility, however, is 1.8 cm^2/V·sec. This is much lower than results obtained from Hall measurements at room temperature of similar unprocessed samples [14]. This is also consistent with Coulomb scattering that could be due to gap states introduced as a result of WO_{3-x} reduction during the device fabrication process [18]. The reduction in resistance that is observed as the temperature drops could be due to an insulator-to-metal transport transition recently reported by Mattoni et al. in WO_{3-x} [19]. This would also result in a reduced work function and degraded surface transfer doping efficiency at room temperature [18].

Our results reveal the potential of the D:H/WO_3 system for future transistor applications but also illustrate the challenge of maintaining high TMO quality during device fabrication, an issue already noted in [11]. To exploit the advantageous properties of the D:H/TMO system, transistor fabrication processes will need to be developed that maintain the integrity of the TMO layer.

IV. CONCLUSIONS

We demonstrate for the first time p-type Diamond:H/WO_3 FETs. Long-channel devices display well behaved transistor characteristics with 10^3 ON-OFF ratio at room temperature. An anomalous threshold voltage dependence on WO_3 thickness is observed which is consistent with enhanced surface transfer doping as the WO_3 layer is thinned down. Low-temperature mobility measurements suggest strong Coulomb scattering perhaps due to WO_3 degradation during the fabrication process.

ACKNOWLEDGMENT

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